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PATENT 5732-00300/MA-069

## N THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of:

Verma et al.

Serial No. 10/080,036

Filed: February 19, 2002

For:

MEMORY MODULE HAVING

INTERCONNECTED AND STACKED

INTEGRATED CIRCUITS

Group Art Unit: 2827 Examiner: Luan C. Thai

Atty. Dkt. No. 5732-00300

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the date indicated below:

September 29, 2003

Date

## AMENDMENT; RESPONSE TO OFFICE ACTION MAILED JULY 1, 2003

## **Box Non-Fee Amendment**

Assistant Commissioner of Patents and Trademarks Washington, D.C. 20231

Dear Sir/Madam:

This paper is submitted in response to the Office Action of July 1, 2003, to further highlight reasons why the captioned application is in condition for allowance. The undersigned wishes to thank Examiner Thai for the courtesies extended during an interview of September 29, 2003. In that interview, the patentability of the pending independent claims 1 and 9 was discussed in light of the Office Action §103(a) rejection. The interview dealt primarily with applicants traversal of the §103(a) rejection since the Office Action failed to establish a *prima facie* case of obviousness. Nowhere in either of the cited references is there any suggestion or motivation for the hypothetical combination proposed in the Office Action. MPEP 2143.01. However, to expedite prosecution of this case, applicants request the following amendments to place this case in condition for early allowance:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.